

## CLAIMS

What is claimed is:

*SUB A4*

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1. A method for fabricating a silicide for a semiconductor device, said method comprising:  
depositing a metal or an alloy thereof on a silicon substrate;  
reacting said metal or said alloy to form a first silicide phase;  
etching any unreacted metal or alloy;  
depositing a silicon cap layer over said first silicide phase;  
reacting the silicon cap layer to form a second silicide phase, for said semiconductor  
device; and  
etching any unreacted silicon.

2. The method of claim 1, wherein said substrate comprises a bulk silicon substrate.

3. The method of claim 1, wherein said substrate comprises a silicon-on-insulator (SOI)  
substrate.

*SUB AS*

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4. A method for fabricating a silicide for a silicon region, said method comprising:  
depositing a metal or an alloy thereof on a bulk silicon substrate;  
reacting said metal or said alloy to form a first silicide phase;  
etching any unreacted metal or alloy;

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depositing a silicon cap layer over said first silicide phase;  
reacting the silicon cap layer to form a second silicide phase; and  
etching any unreacted silicon.

5. The method of claim 4, wherein said depositing of said metal comprises performing a blanket

5 deposition of a metal comprising one of Co, Ti and Ni.

6. The method of claim 5, wherein said blanket deposition includes cobalt having a film

thickness in a range of approximately 7 nm to approximately 8 nm.

7. The method of claim 6, wherein said deposition is followed by a TiN or W cap deposition for preventing oxidation during a subsequent anneal processing.

8. The method of claim 4, further comprising:

10 performing a first rapid thermal anneal (RTA) to form a metal-silicon phase, such that the deposited metal with the underlay Si, converts some of the Si into metal-Si;

selectively etching any unreacted metal, thereby leaving the metal-silicon regions intact;

15 performing a blanket deposition of a silicon film; and

performing a second RTA to form a metal di-silicide.

9. The method of claim 8, wherein when said metal is nickel, said second RTA is omitted.

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10. The method of claim 4, wherein said metal is co-deposited with silicon.

11. The method of claim 10, wherein said metal is cobalt, and a mixture co-deposited is  $\text{Co}_{1-x}\text{Si}_x$ , with  $x < 0.3$ .

12. The method of claim 4, wherein said method forms a raised source-drain structure by a  
5 blanket deposition which uses processing other than epitaxial processing.

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13. A method for fabricating a silicide, said method comprising:  
providing a substrate having a silicon layer;  
depositing a metal or an alloy over said silicon layer;  
reacting said metal or said alloy to form a first silicide phase;  
etching any unreacted metal or alloy; and  
depositing a silicon cap layer over said metal or said alloy;  
reacting the silicon cap layer, to form a second silicide phase; and  
etching any unreacted silicon.

14. A semiconductor device, comprising:

15 a silicon substrate; *A*  
a raised source-drain structure, including a silicided portion formed with an amorphous  
silicon, formed on said substrate without selective epitaxy processing,

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said raised source-drain structure having a surface which is facet-free and has a crystallographic shape which is arbitrary.

15. The device of claim 14, wherein said substrate comprises a bulk silicon substrate.

16. The device of claim 14, wherein said substrate comprises a silicon-on-insulator (SOI) 5 substrate.

17. The device of claim 14, wherein said silicided portion includes a metal comprising one of Co, Ti and Ni.

18. The device of claim 17, wherein said metal includes cobalt having a film thickness in a range of approximately 7 nm to approximately 8 nm.

19. The device of claim 18, wherein a W cap is formed on said metal for preventing oxidation during a subsequent anneal processing.

20. The device of claim 18, wherein a TiN cap is formed on said metal for preventing oxidation during a subsequent anneal processing.

21. The device of claim 14, wherein said raised source-drain structure is free of crystal 15 orientation constraints.

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22. The device of claim 14, wherein said raised source-drain structure is non-aligned with a crystallographic direction of said substrate.

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